

Quasi-Resonant Flyback PWM Controller

Features

- QR ZVS at switch turn-on
- PFM mode at light load condition
- Controllable built-in PFC power supply
- 130 KHz maximum frequency limit
- Internal minimum off-time for correct switching
- Internal leading edge blanking
- Adaptive slope compensation for constant power output
- On-chip thermal shutdown
- Programmable soft-start
- External latch
- 1A peak current sink/source capability
- Programmable over-voltage protection
- Max. on-time limit
- Max. off-time limit
- SOP-8 and DIP-8 package

Applications

- AC/DC adaptors and open-frame SMPS
- LCD monitor/TV/PC/Set-top box
- Consumer electronics (NB, DVD, etc)
- Offline battery charger

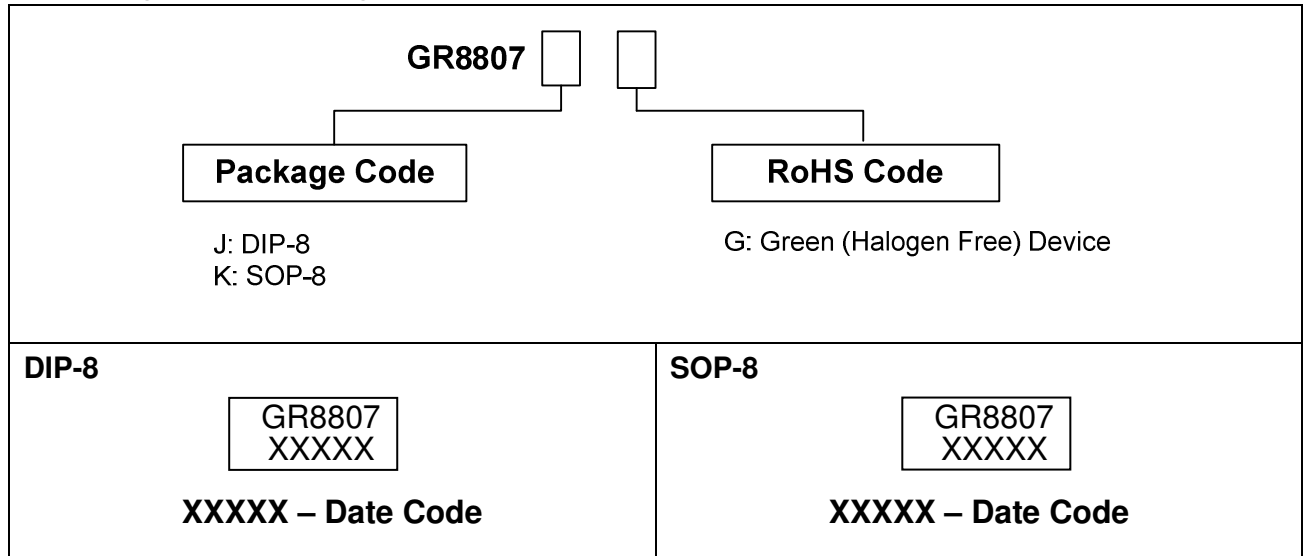
Description

The GR8807 is a standard current mode Quasi-Resonant controller IC, specially designed for high efficiency performance in offline flyback converter applications. In Quasi-Resonant (QR) mode, the MOSFET turn on with its minimum drain voltage by sensing transformer demagnetization. The GR8807 operates in multi-mode. At normal load condition, it works in QR mode while the switching frequency is prevented to exceed the maximum frequency in order to meet the 150 KHz CISPR-22 EMI starting limit. When load gets lighter, efficiency becomes the point. The IC works in PFM mode (fixed on time) to enhance power conversion. Burst mode takes in charge to minimize power consumption and switching loss when no power is needed.

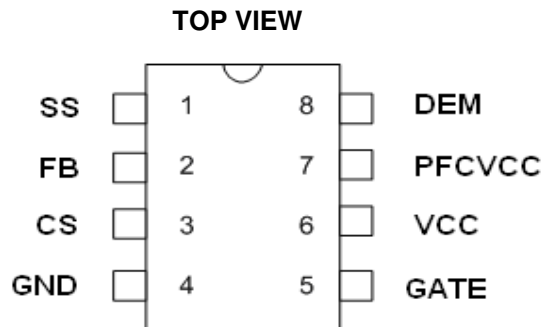
An internal P-channel MOSFET is set up to control the power transferred to PFC IC according to different load conditions.

The GR8807 offers robust and comprehensive protections including under-voltage lockout (UVLO), VCC over-voltage protection (VCC OVP), pulse-by-pulse over-current protection, over-load protection (OLP), output over-voltage protection (Output OVP), built-in thermal shutdown beside VCC clamp, gate clamp, max. on-time Limit, max. off-time limit etc. And programmable soft-start and external latch can be achieved with a few external components.

Ordering and Marking Information



Pin Configuration



Pin Description

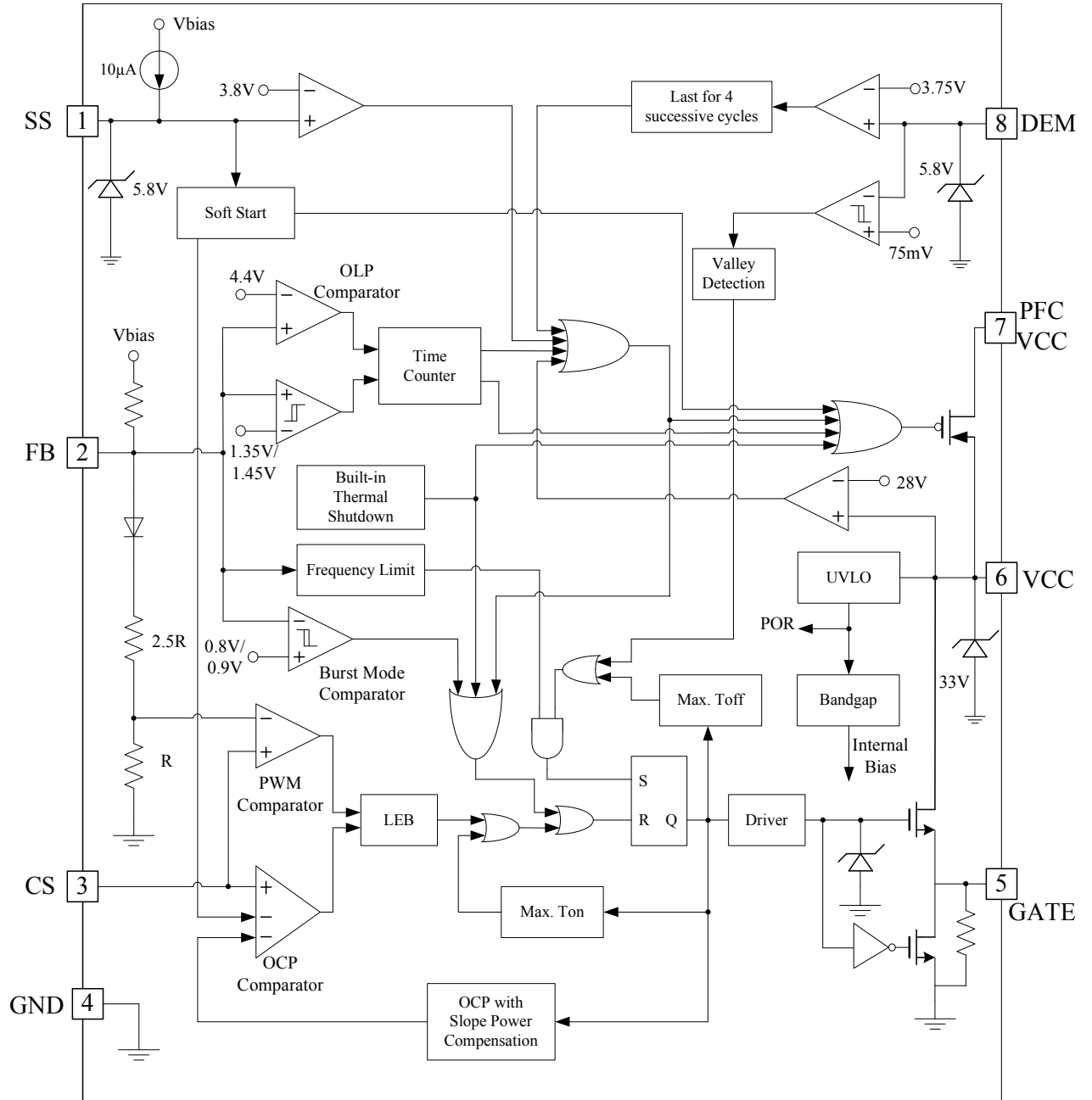
Pin	Symbol	Description
1	SS	Soft-start function and external latch trigger pin.
2	FB	Voltage feedback pin, the PWM duty cycle is determined by this pin voltage and CS pin voltage. And the operation mode is controlled by this pin voltage.
3	CS	Current sense pin, connect to sense the MOSFET current
4	GND	Ground
5	GATE	The output driver for driving the external MOSFET
6	VCC	Power Supply pin
7	PFCVCC	This pin provides power supply to PFC controller in high load condition. The switch between this pin and VCC pin is off during standby or startup sequence.
8	DEM	Transformer core demagnetization detection and output over voltage protection pin.

Absolute Maximum Ratings

Supply voltage VCC, PFCVCC	-----	30V
SS, FB, CS, DEM	-----	-0.3 ~ 6.5V
GATE	-----	-0.3 ~ VCC+ 0.3V
Junction temperature	-----	150°C
Operating ambient temperature	-----	-20°C ~ 85°C
Storage temperature range	-----	-65°C ~ 150°C
SOP-8 package thermal resistance	-----	160°C/W
DIP-8 package thermal resistance	-----	100°C/W
Power dissipation (SOP-8, at ambient temperature = 85°C)	-----	400mW
Power dissipation (DIP-8, at ambient temperature = 85°C)	-----	650mW
Lead temperature (SOP-8 & DIP-8 soldering, 10sec)	-----	230°C
Lead temperature (All Pb free packages, soldering, 10sec)	-----	260°C

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply voltage VCC	11	25	V

Block Diagram


Electrical Characteristics (TA = +25°C unless otherwise stated, Vcc = 16V)

Parameter	Pin	Min.	Typ.	Max.	Unit
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SUPPLY VOLTAGE

Startup current	6	-	10	15	uA
Operating current (VFB = 3V, CS is floating)	6	-	1.8	3.0	mA
Operating current (with 1nF load on Gate pin, VFB = 3V, Fsw = 40KHz)	6	-	2.8	4.0	mA
Current when VCC is latched (VCC = V_latch_release + 1V)	6	-	500	-	uA
UVLO (off)	6	7.5	8.5	9.5	V
UVLO (on)	6	14.0	15.0	16.0	V
OVP level on VCC pin	6	26	28	30	V
VCC Zener clamp voltage	6	31	33	35	V
VCC latch release voltage	6	-	6	-	V

VOLTAGE FEEDBACK

Short circuit current, VFB = 0V	2	-	1.5	-	mA
Open loop voltage, FB pin open	2	-	5.6	-	V
OLP trip level	2	4.27	4.40	4.62	V
PFM mode on threshold voltage	2	1.38	1.45	1.52	V
PFM mode off threshold voltage	2	1.28	1.35	1.42	V
Burst mode on threshold voltage	2	0.85	0.90	0.95	V
Burst mode off threshold voltage	2	0.76	0.80	0.84	V
PFC go to standby threshold voltage	2	1.05	1.1	1.15	V
PFC leave standby threshold voltage	2	1.14	1.2	1.26	V
OLP delay time	2	65	80	100	mS

CURRENT SENSING

Current limiting threshold voltage at zero duty cycle	3	0.43	0.45	0.47	V
Current limiting threshold voltage at 60% duty cycle	3	0.776	0.800	0.824	V
Leading-edge blanking time	3	250	350	550	nS
Delay to output	3	-	120	160	nS

DEMAGNETIZATION DETECTION

Demagnetization comparator trigger voltage	8	10	75	150	mV
Hysteresis voltage for DEM trigger comparator	8	-	20	-	mV
Low state clamp voltage	8	-	-0.7	-	V
High state clamp voltage	8	-	5.8	-	V
Suppression time of the transformer ringing at start of secondary stroke	8	1.5	2	2.5	uS



Interval time after last demag transistion	8	4	5	6	uS
Propagation delay of demag	8	-	160	-	nS
OVP level at DEM pin	8	-	3.75	-	V
Pulse cycles number when true OVP at DEM pin	8	-	4	-	Cycle

SOFT START

Soft start charge current	1	8	10	12	uA
Voltage when soft start is over	1	-	2.2	-	V
Maximum sink current at high state clamp	1	80	140	200	uA
High state clamp voltage	1	-	5.8	-	V
Latch trigger threshold voltage at SS pin (Iss > 200uA)	1	3.42	3.80	4.18	V

PFC ON/OFF

On-resistance of the switch between PFCVCC pin and VCC pin	7	-	20	-	Ω
PFC go to standby delay time	7		120		mS
PFC ON propagation delay time	7	0.5	1	1.5	mS

OSCILLATOR

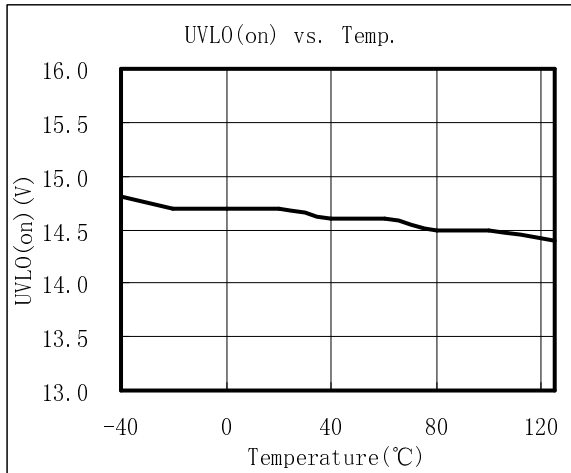
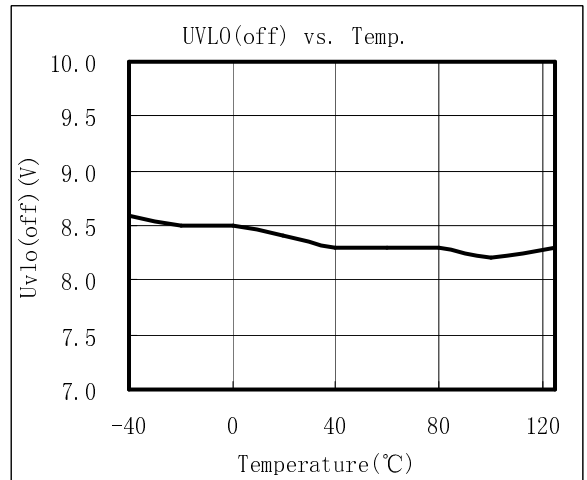
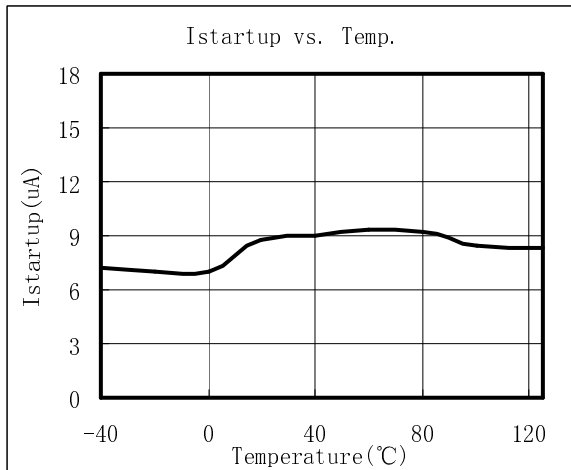
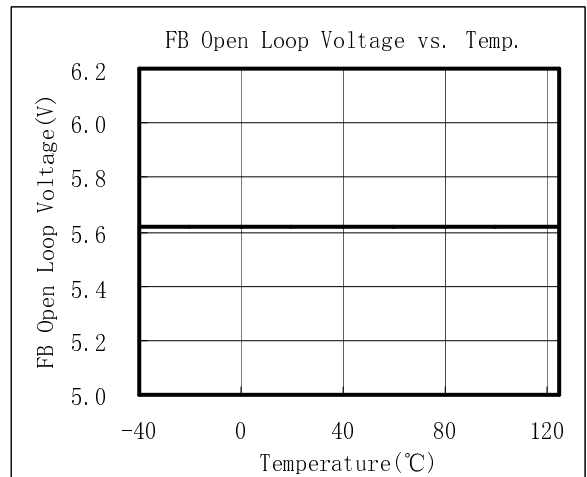
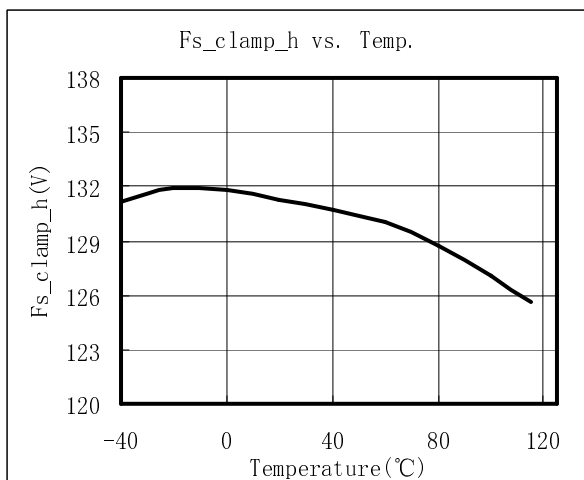
Maximum frequency limit in QR mode		117	130	143	KHz
Burst mode frequency		18	22	-	KHz
Maximum turn on time		16	20	25	uS
Maximum turn off time		55	70	90	uS
Frequency modulation slope versus FB voltage in PFM mode		-	240	-	KHz/V

GATE DRIVE OUTPUT

Output low level (Io = 100mA, sink)	5	-	-	1	V
Output high level (Io = 100mA, source)	5	7.5	-	-	V
Gate clamp voltage (VCC = 20V)	5	-	16.5	-	V
Rising time, load capacitance = 1000pF	5	-	70	-	nS
Falling time, load capacitance = 1000pF	5	-	20	-	nS

OTP

OTP trip level		-	140	-	°C
OTP recovery hysteresis		-	30	-	°C

Typical Performance Characteristics

Fig.1

Fig.2

Fig.3

Fig.4

Fig.5

Application Information

Overview

The GR8807 implements a standard current mode system where the on-time is determined by the peak current setpoint whereas the core demagnetization triggers the pwm to turn on, which is the representative operation mode named Quasi-Resonant. QR converter presents much better power conversion efficiency and EMI performance than traditional fixed switching frequency converter.

The built-in PFC controller makes the GR8807 be a highly integrated solution for efficient power supplies with better power saving and lower cost.

Startup

The GR8807 needs such a low startup current that the capacitor of VCC may be charged up quickly. As a result, a large value resistor can be used to minimize the power dissipation on it.

Multi-Mode Operation

The GR8807 presents three different operations in order to improve power conversion performance by sensing FB voltage, which means input line voltage and needed power at that time.

- When $V_{FB} > 1.45V$, which means normal load condition, the system works in QR mode. The switching frequency increases while load gets low, which is a typical state for Quasi-Resonant. The system operates in DCM. System design should be optimized to get the switching frequency neither too high nor too low.
- When $1.45V > V_{FB} > 1.35V$, the operation mode is the same as the status before.
- When $1.35V > V_{FB} > 0.9V$, which means light load condition, the system works in PFM (Pulse Frequency Modulation) mode to keep in

high power conversion efficiency. Off-time is modulated depending on FB voltage in PFM mode whereas On-time is fixed by internal preset current setpoint. The limited maximum frequency decreases when loading gets lighter. However, the turn-on event is still triggered at the valley of ringing in PFM mode, which implies that the system skips more and more valleys while loading is reduced.

- When $0.9V > V_{FB} > 0.8V$, which means standby or very light load condition, the system works in Burst mode. The MOSFET is always turned off except when V_{FB} goes back up to 0.9V or VCC voltage drops below 0.8V. The switching frequency is fixed to the minimum frequency 22 KHz in order to prevent bringing in audio noise.

Current Sensing and Leading Edge Blanking

The primary current is monitored through a sense resistor between Source pin of Power MOS and the GND pin. The sense voltage on the resistor and the FB input voltage determine the PWM duty cycle, and pulse-by-pulse OCP allows the maximum output power. Leading edge blanking circuit is built-in to prevent mistaken turn-off event, which is due to snubber diode reverse recovery during initial MOSFET on state. So external RC filter is no longer needed.

Demagnetization Detection

When the controller instructs the switch opening, the drain voltage quickly rises and the energy transfer between primary and secondary takes place: the secondary diode conducts and the output voltage flies back on the primary side. During this time, the primary current decreases with a slope determined by the reflected output voltage and primary inductance. When the primary current

reaches zero, the transformer core is fully demagnetized. As a result, a natural oscillation occurs, exhibiting the following frequency value:

$$F_{ring} = 1/(2\pi\sqrt{L_p C_d})$$

where L_p is the primary inductance and C_d is the capacitance on the drain node including all the parasitic capacitance and stray capacitance.

As in any sinusoidal signal, there are peaks and valleys. When you restart the switch in one valley, where the voltage is minimum, the MOSFET is no longer the seat of heavy turn-on loss engendered by capacitive effects: this is the so-called Quasi-Resonant operation. The switching frequency depends on the peak current, the various slopes and the number of valleys you choose after the core reset.

The core reset detection is done by monitoring the voltage activity on the auxiliary winding through DEM pin. This voltage features a FLYBACK polarity.

Demagnetization is detected when the voltage at DEM is below a fixed value (typically 75 mV) in falling edge, nevertheless the detection is suppressed during the first suppression time, which is necessary especially when the transformer has a large leakage inductance or during the startup.

Ringings Suppression Timer

In applications where the transformer has a large leakage inductance especially when output voltage is low or startup is activated, mistaken turn-on event is inevitable without ringing suppression timer. When current setpoint is reached, ringing suppression timer starts and prevents the switch from turning on during the suppression time.

Maximum and Minimum On-time

The minimum on-time is determined by internal LEB

time. The controller limits the on-time to a maximum of 20us in order to protect external power device, for instance, the MOSFET.

Maximum Frequency Limit

In QR mode, the frequency increases as the load decreases. Therefore, to meet the CISPR-22 EMI limit starting at 150 KHz, the maximum frequency is limited to 130 KHz.

PFC VCC Power On/Off Controller

Due to the built-in low resistance P-channel MOSFET and PFC logic controller, PFC converter could be powered by PWM auxiliary power supply. PFCVCC is shutdown when load is not high enough or during soft-start. To prevent any damage, PFCVCC is also shutdown in any of following conditions: VCC OVP, OLP, Output OVP, External Latch Trigger, and Internal Thermal Shutdown.

External Latch Triggering

GR8807 provides a latch trigger voltage level at SS pin. The IC enters a permanent latch-off phase and stops all switching operations if the SS voltage is higher than 3.8V, and only can be resumed until VCC voltage fall below 6V, which means the user should unplug the power supply from the mains outlet. This latch trigger could meet separate user's demand.

Over Load Protection

In applications where the load is purposely not controlled, it is necessary to implement a over load protection, which actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the VFB is pulled up to its open voltage, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of

feedback loss, e.g. a broken optocoupler. To account for this situation, GR8807 hosts a dedicated overload detection circuitry. Once the FB pin level reaches 4.4V and lasts for more than 80ms, this circuitry imposes to deliver pulses in a burst manner with a low duty cycle. The system recovers when the fault condition disappears.

Output Over Voltage Protection

If the secondary-side feedback circuit trouble or a solder defect results in an opening in the feedback path, the current through the optocoupler transistor becomes almost zero. Then, FB voltage climbs up in a manner similar to the over load situation. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection triggers, leading to the breakdown of the devices in the secondary side. To prevent this situation, an output OVP circuitry is employed.

In general, the peak voltage of the DEM signal is proportional to the output voltage, so the GR8807 uses a DEM signal instead of directly monitoring the output voltage. If the DEM signal exceeds 3.75V, an output OVP is triggered, shutting down the converter. To avoid undesired trigger during normal operation, there are two points to be considered. One is the sampling at the DEM pin should begin after a 2 μ s preset delay during the flyback phase to make sure the leakage inductance ringing has been fully damped, and the other is that OVP events should be detected in successive 4 cycles in order to avoid possible ESD or Surge events. If the OVP events detected last less than 4 successive cycles, the counter resets and no protective action occurs.

Programmable Soft-start

The GR8807 features an internal soft-start to soften the constraints occurring in the power supply during

startup. It is activated during the power on sequence. As soon as VCC reaches UVLO on, an internal trimmed 10 μ A current flow into the external capacitor connected with SS pin. The peak current is gradually increased until SS voltage reaches 2.2V, which implies that soft-start is over. Every restart attempt is followed by a soft-start activation.

SS pin is also used for external latch triggering (Please refer to “External Latch Triggering” section).

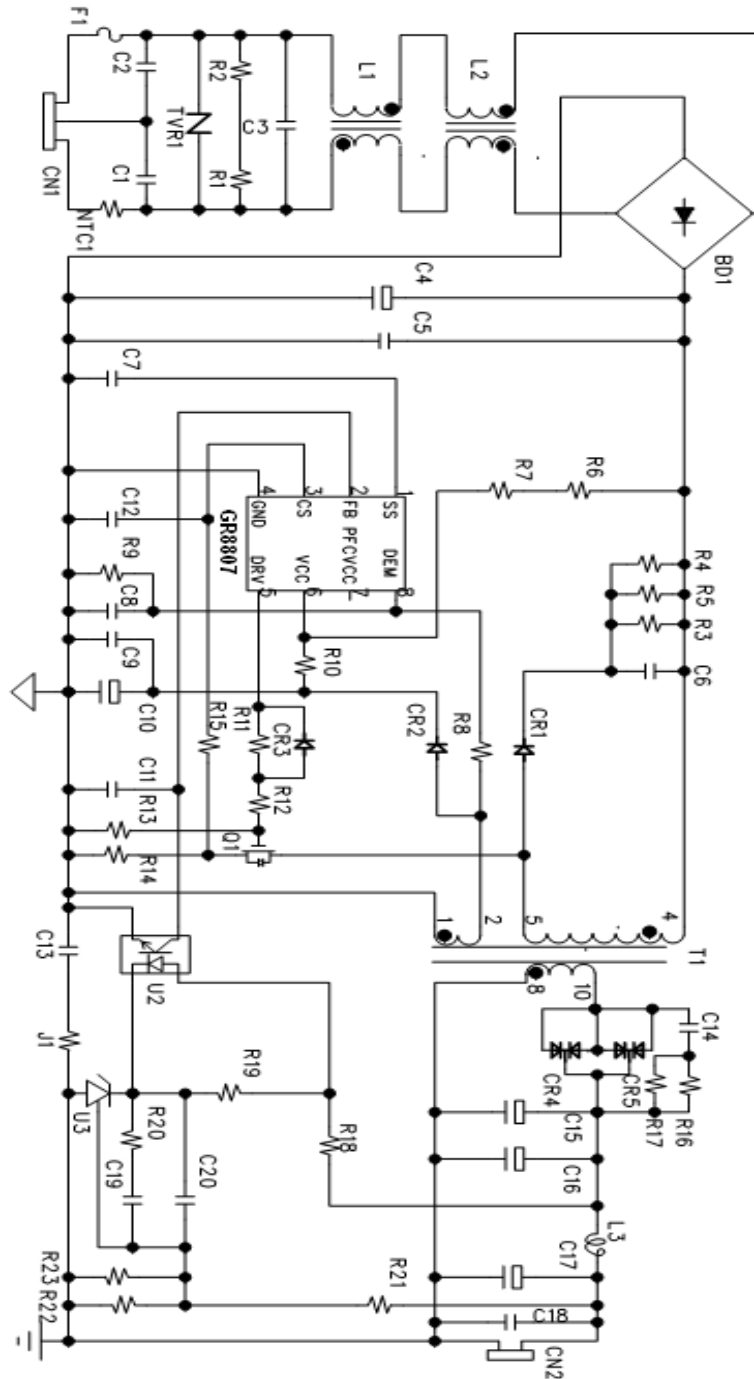
Gate Drive and Clamp

A totem pole buffer, with 1A peak source and sink capability, drives the external MOSFET. It has a built-in circuitry to inhibit conduction on both high-side MOSFET and low-side MOSFET at the same time. An internal 16.5V clamp is added to protect the external transistor switch against undesirable over voltage. The output is active HIGH and at VCC voltage below the UVLO on, the gate drive is internally pulled low to maintain the off state.

On-chip Thermal Shutdown

To prevent permanent damage caused of high junction temperature, the IC will stop switching and resume operation when the junction temperature decreases by 30°C.

Typical Application Circuit

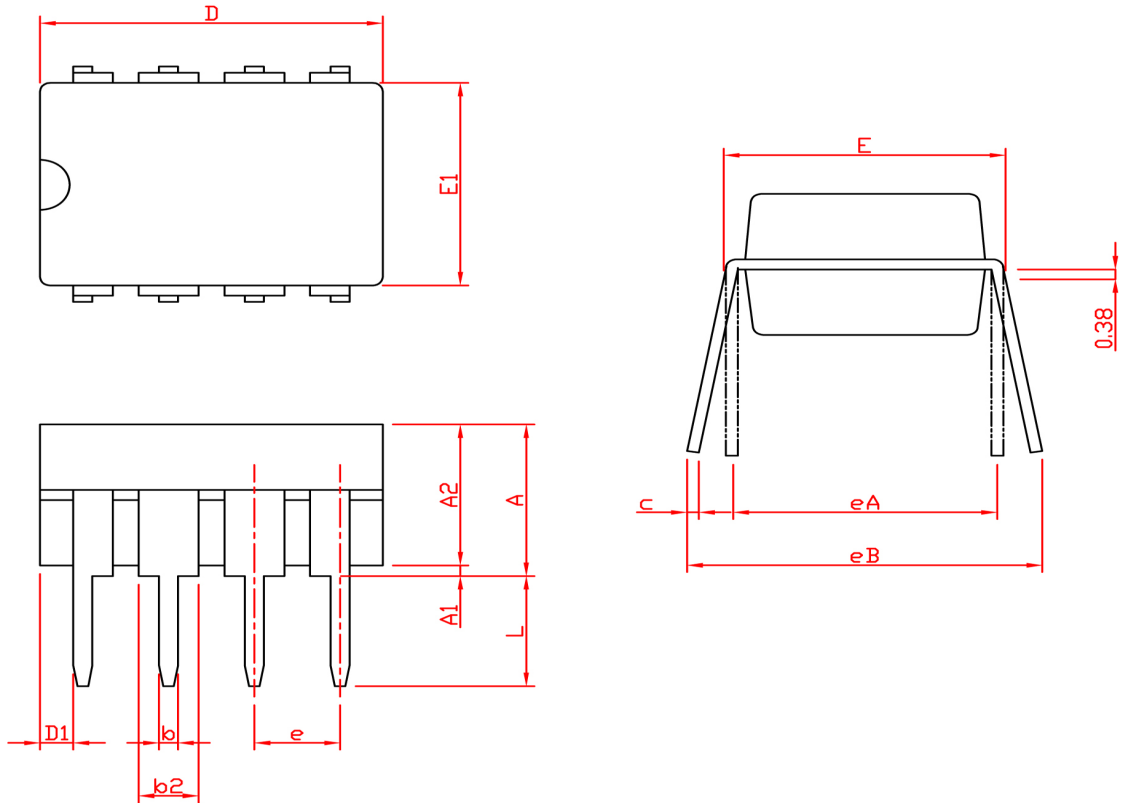


Bom List

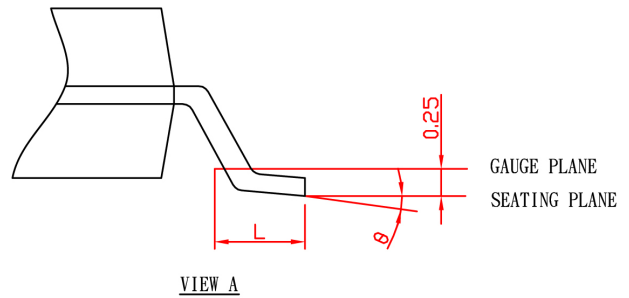
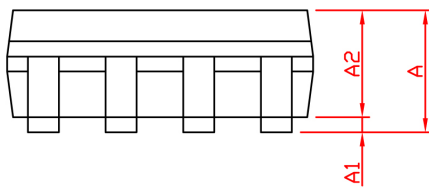
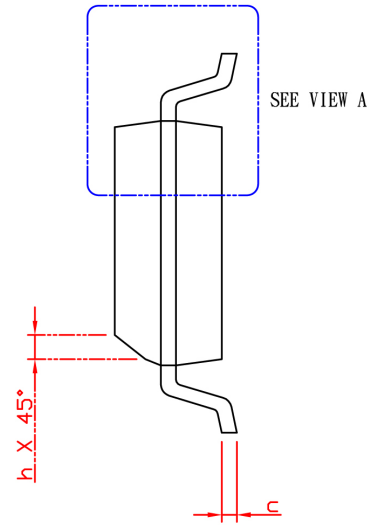
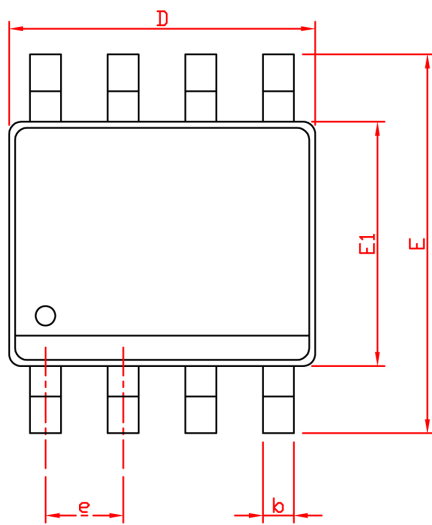
No.	Part. No	Description	Note
1	BD1	KBL406	
2	C1	Y2-CAP/CS102	
3	C2	Y2-CAP/CS102	
4	C3	X2-CAP/0.22uF	
5	C4	E-CAP, 400V/120uF	
6	C5	DIP, 103/1KV	
7	C6	DIP, 103/1KV	
8	C7	SMD0805, 103	5%
9	C8	SMD0805, 22P	5%
10	C9	SMD0805, 103	5%
11	C10	E-CAP 50V/10uF	
12	C11	N.A.	
13	C12	SMD0805, 102	5%
14	C13	Y1-CAP CD222	
15	C14	DIP, 222/1KV	
16	C15	E-CAP 25V/680uF	
17	C16	E-CAP 25V/680uF	
18	C17	E-CAP 25V/100uF	
19	C18	SMD0805, 105	5%
20	CN1	AC Connector	
21	CR1	DO-41, FR107	
22	CR2	DO-41, FR104	
23	CR3	DO-80, 1N4148	
24	CR4	TO220,	
25	CR5	TO220,	
26	F1	2010, 250V/3.15A	
27	HS1	Heat sink	
28	HS2	Heat sink	
29	L1	GRT181007-103M-	10mH
30	L2	GRT120604-501M-	0.5mH
31	L3	GR0315-1R6M-N	1.6uH
32	NTC1	5Ω	

No.	Part. No	Description	Note
33	PCB	GR0705702	
34	Q1	FQPF10N60C	
35	R1	SMD1206, 105	5%
36	R2	SMD1206, 105	5%
37	R3	SMD1206, 204	5%
38	R4	SMD1206, 204	5%
39	R5	SMD1206, 204	5%
40	R6	SMD1206, 754	5%
41	R7	SMD1206, 105	5%
42	R8	SMD0805, 124	5%
43	R9	SMD0805, 333	5%
44	R10	SMD0805, 3.9R	5%
45	R11	SMD0805, 33R	5%
46	R12	SMD0805,10R	5%
47	R13	SMD0805,103	5%
48	R14	DIP,1W / 0.20Ω	
49	R15	SMD1206, 101	5%
50	R16	SMD1206, 22R	5%
51	R17	SMD0805, 102	5%
52	R18	SMD0805, 471	5%
53	R19	N.A.	
54	R20	SMD0805, 203	5%
55	R21	SMD0805, 333	1%
56	R22	SMD0805, 183	1%
57	R23	SMD0805, 682	1%
58	T1	POT3019	
59	TVR1	10471	
60	U1	GR8807	SOP-
61	U2	PC123	
62	U3	TL431	
63	J1	SMD0805, 0R	5%

Package Information



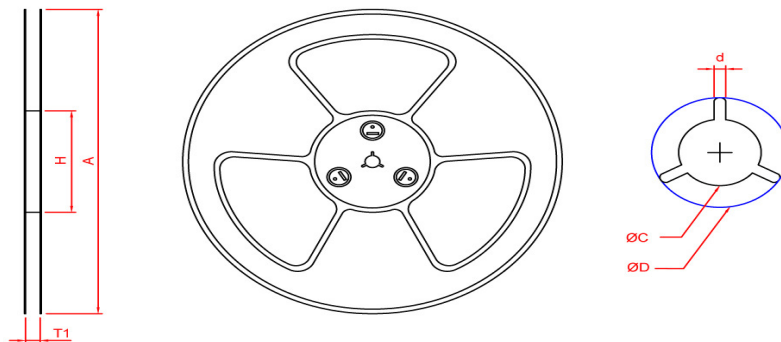
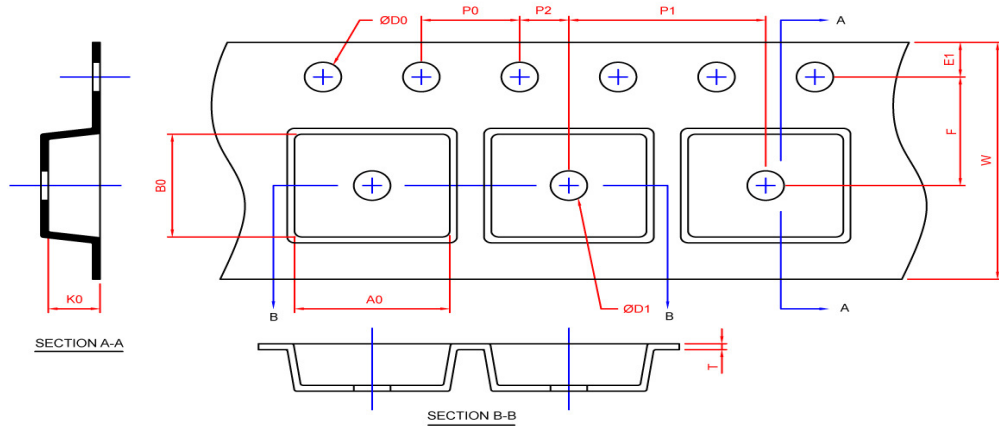
SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Package Information


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Carrier Tape & Reel Dimensions

SOP-8



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.0	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP-8	12	-	2500

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